What is claimed is:

1. A method for synchronizing incoming data received by a chip, comprising steps of:

first sampling the incoming data on an active transition edge of a first cycle of a clock to produce a sample A;

second sampling the incoming data on the active transition edge of a second cycle of the clock, the second cycle being previous to the first cycle to produce a sample B;

third sampling the incoming data on an inactive transition edge of the second cycle of the clock to produce a sample C;

fourth sampling the incoming data on the inactive transition edge of a third cycle of the clock, the third cycle being previous to the second cycle to produce a sample D; and

delaying the incoming data by an amount depending upon A, B, C, and D.

2. The method of claim 1, wherein the active transition edges are rising edges.

3. The method of claim 1, wherein the step of delaying includes delaying the incoming data by such an amount that transition edges of the incoming data occur in synchronization with the inactive transition edges of the clock.

4. The method of claim 1, wherein the step of delaying includes sequentially incrementing, decrementing, or maintaining the amount of delay for each of a plurality of cycles of the clock.

5. The method of claim 4, wherein incrementing and decrementing are performed in steps of 1/16 of the clock cycle.

6. The method of claim 4, wherein incrementing and decrementing are performed in steps of 1/32 of the clock cycle.

7. The method of claim 1, further including a step of initially delaying the incoming data by an initial amount prior to the step of delaying, the initial amount depending upon a length of the clock cycle.

8. The method of claim 1, further including a step of initially delaying the incoming data by an initial amount of approximately 0.75 of the clock cycle prior to the step of delaying.

9. The method of claim 1, wherein the step of delaying includes decrementing the amount of delay responsive to ABCD equaling 1000, 0111, X010, X101, X100, or X011, and incrementing the amount of delay responsive to ABCD equaling X110 or X001.

10. The method of claim 9, wherein the step of delaying further includes maintaining the amount of delay responsive to ABCD equaling 0000 or 1111.

11. A method for adjusting for latency in a chip-to-chip link, comprising steps of:

defining an expected latency associated with the link;

sending a starter signal to a first chip and a second chip;

responsive to the first chip receiving the starter signal, the first chip sending a latency adjustment signal to the second chip over the link;

the second chip measuring a latency between the second chip receiving the starter signal and the second chip receiving the latency adjustment signal;

the second chip comparing the measured latency with the expected latency; and

the second chip adding a delay such that the measured latency matches the expected latency.

12. A circuit for measuring synchronization of incoming data to a chip in comparison with a clock, comprising:

a first register having an input coupled to the incoming data and an output, and configured to temporarily hold at the output a value of the incoming data received at active transition edges of the clock;

a second register having an input coupled to the incoming data and an output, and configured to temporarily hold at the output a value of the incoming data received at inactive transition edges of the clock;

a third register having an input coupled to the output of the first register and an output, and configured to temporarily hold at the output a value of the output of the first register received at active transition edges of the clock;

a fourth register having an input coupled to the output of the second register and an output, and configured to temporarily hold at the output a value of the output of the second register received at active transition edges of the clock; and

a fifth register having an input coupled to the output of the fourth register and an output, and configured to temporarily hold at the output a value of the output of the fourth register received at active transition edges of the clock.

13. The circuit of claim 12, further including a delay circuit portion configured to delay the incoming data and to alter the delay of the incoming data depending upon the outputs of the first, third, fourth, and fifth registers.

14. The circuit of claim 12, further including a delay circuit portion configured to delay the incoming data and to increment, decrement, or maintain the delay of the incoming data depending upon the outputs of the first, third, fourth, and fifth registers.

15. A system on a chip for synchronizing incoming data with a clock, comprising:

a sampling portion configured to sample the incoming data at transition edges of the clock;

a decision portion coupled to the sampling portion and configured to decide whether to increase, decrease, or maintain the delay amount based on an output of the sampling portion; and

a programmable delay portion coupled to the decision portion and configured to delay the incoming data by the delay amount.

16. The system of claim 15, further including a smoothing portion coupled to the decision portion and the programmable delay portion and configured to increase, decrease, or maintain the delay amount based on at least two sequential decisions by the decision portion.

17. A receiver circuit on a chip, comprising:

a digital phase adjustment unit configured to adjust a delay of incoming data to the chip, the digital phase adjustment unit periodically increasing and decreasing the delay depending upon values of the incoming data at transition edges of a clock;

a latency adjustment unit coupled to the digital phase adjustment unit, configured to adjust for a difference between an expected latency of the incoming data and an actual latency of the incoming data; and

a controller configured to control operations of the digital phase adjustment unit and the latency adjustment unit.

18. The receiver circuit of claim 17, further including a feedback loop between an output and an input of the digital phase adjustment unit, the digital phase adjustment unit using the feedback loop to determine an initial amount of the delay.

19. The receiver circuit of claim 18, wherein the initial amount of delay depends upon a period of the clock.

20. The receiver circuit of claim 18, wherein the initial amount of delay is approximately 0.75 of a period of the clock.

21. The receiver circuit of claim 17, wherein the digital phase adjustment unit includes a sampler configured to sample the values of the incoming data at an active transition edge of a first cycle of the clock to produce a value A, at the active transition edge of a second cycle of the clock, the second cycle being previous to the first cycle to produce a value B, at an inactive transition edge of the second cycle of the clock to produce a value C, and at the inactive transition edge of a third cycle of the clock, the third cycle being previous to the second cycle to

produce a value D, wherein the digital phase adjustment circuit increases and decreases the delay based on the values A, B, C, and D.

22. The receiver circuit of claim 17, wherein the controller is configured to send a message to the latency adjustment unit, the message including a value of the expected latency.

23. The receiver circuit of claim 17, wherein the digital phase adjustment unit includes a pointer that points to an amount of the delay, the pointer moving as the delay is increased and decreased.

24. The receiver circuit of claim 17, wherein the controller is configured to control the digital phase adjustment unit to generate an initial amount of the delay and to control the latency adjustment unit to adjust for latency.